

CLAIMS

1 1. A semiconductor structure comprising:
2 a substrate;
3 a lattice-mismatched first layer deposited on said substrate and annealed at a temperature
4 greater than 100°C above the deposition temperature; and
5 a second layer deposited on said first layer with a greater lattice mismatch to said
6 substrate than said first layer.

1 2. The semiconductor structure of claim 1, wherein said substrate comprises Si and said
2 first and second layers comprise $Si_{1-x}Ge_x$.

1 3. The semiconductor structure of claim 1, wherein said substrate has a surface layer
2 comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

1 4. The semiconductor structure of claim 1, wherein said substrate comprises GaAs and
2 said first and second layers comprise $In_yGa_{1-y}As$.

1 5. The semiconductor structure of claim 1, wherein said substrate has a surface layer
2 comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

1 6. The semiconductor structure of claim 1, wherein said substrate comprises GaP and
2 said first and second layers comprise $In_zGa_{1-z}P$.

1 7. The semiconductor structure of claim 1, wherein said substrate has a surface layer
2 comprising GaP and said first and second layers comprise $\text{In}_z\text{Ga}_{1-z}\text{P}$.

1 8. The semiconductor structure of claim 2, wherein said first and second layers differ by
2 a Ge concentration less than 10% Ge.

1 9. The semiconductor structure of claim 2, wherein said first and second layers differ in
2 Ge concentration by approximately 1.5% Ge.

1 10. The semiconductor structure of claim 2, wherein said first and second layers of Si_1
2 $_{x}\text{Ge}_x$ are deposited at a growth temperature less than 850°C.

1 11. The semiconductor structure of claim 2, wherein said annealing occurs at a
2 temperature greater than 900°C.

1 12. The semiconductor structure of claim 2, wherein anneal time is greater than 0.1
2 seconds.

1 13. The semiconductor structure of claim 2, wherein said first and second layers differ in
2 Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and
3 the anneal temperature is approximately 1050°C.

1 14. The semiconductor structure of claim 2, wherein said first and second layers differ in
2 Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and
3 the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

1 15. The semiconductor structure of claim 1, wherein said lattice-mismatched
2 semiconductor layer is deposited by chemical vapor deposition.

1 16. A semiconductor graded composition layer structure on a semiconductor substrate

2 comprising:

3 a semiconductor substrate;

4 a first semiconductor layer having a series of lattice-mismatched semiconductor layers

5 deposited on said substrate and annealed at a temperature greater than 100°C above the
6 deposition temperature;

7 a second semiconductor layer deposited on said first semiconductor layer with a greater

8 lattice mismatch to said substrate than said first semiconductor layer, and annealed at a

9 temperature greater than 100°C above the deposition temperature of said second semiconductor
10 layer.

1 17. The structure of claim 16, wherein said substrate comprises Si and said first and
2 second layers comprise SiGe.

1 18. The structure of claim 16, wherein said substrate has a surface layer comprising Si

2 and said first and second layers comprise $\text{Si}_{1-x}\text{Ge}_x$.

1 19. The structure of claim 16, wherein said substrate comprises GaAs and said first and
2 second layers comprise $\text{In}_y\text{Ga}_{1-y}\text{As}$.

1 20. The structure of claim 16, wherein said substrate has a surface layer comprising
2 GaAs and said first and second layers comprise $\text{In}_y\text{Ga}_{1-y}\text{As}$.

1 21. The structure of claim 16, wherein said substrate comprises GaP and said first and
2 second layers comprise $\text{In}_z\text{Ga}_{1-z}\text{P}$.

1 22. The structure of claim 16, wherein said substrate has a surface layer comprising GaP
2 and said first and second layers comprise $\text{In}_z\text{Ga}_{1-z}\text{P}$.

1 23. The structure of claim 17, wherein sequential layers in the graded composition layers
2 differ by a Ge concentration less than 10% Ge.

1 24. The structure of claim 17, wherein sequential layers in the graded composition layers
2 differ in Ge concentration by approximately 1.5% Ge.

1 25. The structure of claim 17, wherein said first and second layers are deposited at a
2 growth temperature of less than 850°C.

1 26. The structure of claim 17, wherein said annealing occurs at a temperature greater
2 than 900°C.

1 27. The structure of claim 17, wherein anneal time is greater than 0.1 seconds.

1 28. The structure of claim 17, wherein sequential layers in the graded composition layers
2 differ in Ge concentration by approximately 1.5%, the growth temperature is approximately
3 750°C, and the anneal temperature is approximately 1050°C.

1 29. The structure of claim 17, wherein sequential layers in the graded composition layers
2 differ in Ge concentration by approximately 1.5%, the growth temperature is approximately
3 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than
4 0.1 seconds.

1 30. The semiconductor structure of claim 16, wherein said lattice-mismatched
2 semiconductor layer is deposited by chemical vapor deposition.